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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/008,531	01/16/1998	HOWARD E. RHODES	MIO012V2	6336

7590 05/22/2006

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ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/22/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/008,531
Filing Date: January 16, 1998
Appellant(s): RHODES, HOWARD E.

Susan M. Luna
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 03, 2006 appealing from the Office action mailed October 05, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is substantially correct. No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct as to Figures 4-7.

In addition, Figures 8-9, as described in specification page 11, lines 5-29, show "*the localized thick region is formed as a spacer*" 34 (as recited in claims 23 and 22), in which a contact hole is etched in the over layer 28 and in an overetch amount into but not through the substantially vertical component 34 of the layer of conductive material in the opening (claims 23,22,21).

Additionally, Figures 15-16, as described in the specification page 9, line 29 through page 14, show "a structure having an opening *in* said at least one *semiconductor* layer" 58 as recited in claim 31 while Figures 4-7 do not show "a structure having an opening *in* said at least one semiconductor layer", in which, as shown in Figure 15, a contact hole 92 is formed in the overlayer 88 and extending into the vertical component 86 of the layer 80 of conductive material, the contact hole disposed adjacent to and directly contacting the vertical component 86 in the opening (Figs 14-16).

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTION

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner as cumulative.

(4) Claims 21-22, 24, and 31-32 as rejected under 35 U.S.C. 103(a) as being unpatentable over Bergemont (US 5,484,741) taken with Toshiyuki et al. (JP-05-109905) and Zamanian (US 5,793,111).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,563,089	JOST ET AL.	2-1995
5,459,094	JUN	10-1995

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

** Claims 31-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 31 recites the limitation "said overlayer having a thickness greater than said underlayer" . There is insufficient antecedent basis for this limitation in the claim. Dependent claim 32 is rejected as depending on rejected indefinite base claim 31.

Claim Rejections - 35 USC § 102

** Claims 21,22,23,25 are rejected under 35 U.S.C. 102(e) as being anticipated by Jost et al (5,563,089).

Jost et al '089 teach (at Figs 10-12; col 5, line 37 through col 6) a method for forming a semiconductor device comprising at least the steps of: providing a substrate 11 having at least one semiconductor substrate layer 11 or polysilicon gates 12,14,16 (Fig 10; Fig 1, col 3, lines 37-50); forming an underlayer 20,28 having an opening over the at least one semiconductor layer; forming a layer 40 of conductive material over the underlayer 20,28 and in the opening, the layer 40 of conductive material having a topography that includes a substantially vertical component in the opening of the underlayer 20,28 (Fig 1, col 3, line 37 through col 4; Fig 10; col 5, lines 37-65; and Figs 1-6, col 3, line 38 through col 5); forming an overlayer 44a over the layer 40 of conductive material (Fig 10), the overlayer 44a having a thickness greater than the underlayer 20 (Fig 11); etching a contact hole in the overlayer 44a and in an overetch amount into but not through of the substantially vertical component of the layer 40 of conductive material in the opening (Fig 11; col 5, lines 51-65; Figs 6-7, col 5, lines 6-26); and forming a contact 46a in the contact hole disposed adjacent to and directly contacting the vertical component (Fig 12). Re claim 22, wherein the vertical component in the opening of the underlayer 28 defines a localized thick region in the layer 40 of conductive material (Figs 10-12). Re claim 23, wherein the vertical component in the layer 40 of conductive material in the opening of the underlayer 28 is a spacer as shown in Figures 10-12. Re claim 25, wherein the conductive layer 40 is a capacitor electrode (Figs 10-12; Figs 5-8; col 4, line 58 through col 5, line 65).

** Claims 21-25,31,32 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun (5,459,094).

Jun teaches (at Figures 4a-4f;8a-8f) a method for forming a semiconductor device comprising at least the steps of: providing a substrate 100 having at least one semiconductor layer (100 or 13; Figs 4a, col 4, lines 45-63, Fig 8a-8f; col 10, line 6 through col 11, line 15) forming an underlayer 12 (Figs 2,4a, col 4, lines 45-63; lines 22-35) of a structure having an

opening 15 over the at least one semiconductor layer 100/13 (Figs 4a,8a; col 5, lines 1-14); forming a layer 16 of conductive material over the under layer and in the opening 15, the layer of conductive material having a topography that includes a substantially vertical component in the opening (Figs 4b,8b; col 5, lines 15-25); forming an overlayer (17 in Fig 4b-4c; 25 in Figs 8b-8c) over the layer 16 of conductive material, wherein the overlayer 17 having a thickness (of about 1000 Angstroms, col 5, lines 26-30) is greater than the underlayer 12 (of thickness of 100-200 angstroms; col 4, lines 55-58); etching a contact hole in the overlayer and in an overetch amount into but not through the substantially vertical component of the layer 16 of conductive material in the opening (Fig 4c;8c; col 5, lines 31-57; col 11, lines 44-55); and forming a contact 19 in the contact hole disposed adjacent to and directly contacting the vertical component (Fig 4e; col 5, line 58 through col 6; Fig 8d-f; col 10, line 59 through col 11). Re claim 22, wherein the vertical component defines a localized thick region in the layer 16 of conductive material (Figs 4a-4f;8a-8f). Re claim 23, wherein the vertical component of the layer 16 of conductive material is a spacer located in the contact hole 15 of the underlayer 14 (Figs 4f,8f). Re claim 24, the method further comprises forming a structure 14 having an opening therein under the conductive layer 16 and filling the opening 14 with the conductive material 16 to form the vertical component (Figs 4a-4f;8a-8f). Re claim 25, wherein the conductive layer 16 is a capacitor electrode (Figs 4a-4f,8a-8f; col 6, lines 15-27). Jun teaches (at Figures 4a-4f;8a-8f) a method for forming a semiconductor device comprising at least the steps of: providing a substrate 100 having at least one semiconductor layer (13; Figs 4a, col 4, lines 45-63, Fig 8a-8f; col 10, line 6 through col 11, line 15) forming an underlayer of a structure having an opening 15 in the at least one semiconductor layer 13 (Figs 4a,8a; col 5, lines 1-14); forming a layer 16 of conductive material over the at least one semiconductive layer 13, and filling the opening 15 with the layer 16 of conductive material to form a substantially vertical component in the opening (Figs 4b,8b; col 5, lines 15-25); forming an overlayer (17 in Fig 4b-4c; 25 in Figs 8b-8c) over the layer 16 of conductive material; forming a contact hole in the overlayer and extending into the vertical component of the layer 16 of conductive material in the opening (Fig 4c;8c; col 5, lines 31-57; col 11, lines 44-55), the contact hole disposed adjacent to and directly contacting the vertical component in the opening; and filling the contact hole with a conductive material 19 (Fig 4e; col 5, line 58 through col 6; Fig 8d-f; col 10, line 59 through col 11). Re claim 32, wherein the

vertical component defines a localized thick region in the layer 16 of conductive material (Figs 4a-4f;8a-8f).

(10) Response to Argument

(1) Rejection of claims 31-32 under 35 U.S.C. 112, second paragraph:

Appellant inquires (at Appeal Brief page 4) that "...given opportunity, they will amend claim 31...".

In response, in the final Office Action mailed October 5, 2005, a shorten statutory period for reply is set to expire 3 months from the mailing date of the final Office Action.

In this Appeal Brief, however, there is no disputing or challenging about the rejection of claims 31-32 under 35 U.S.C. 112, second paragraph, by the appellant. Therefore, the rejection is still outstanding.

Accordingly, it is believed that the rejection should be sustained.

(2) Rejection of claims 21-23 and 25 under 35 U.S.C. 102(e) by using Jost et al. (5,563,089):

** First, Appellant refers to the subject matter as shown in Figures 4-7 of Appellant's application. However, attention is also directed to subject matter as shown in Figures 8-9 of Appellant's application, which subject matter is also corresponding at least to claims 23, 22, and 21. As described in specification page 11, lines 5-29 and shown in Figures 8-9, "*the localized thick region is formed as a spacer*" 34 (see claims 23,22), in which base claim 21 recites etching a contact hole in the overlayer 28 and in an overetch amount into but not through the substantially vertical component 34 of the layer of conductive material in the opening (claims 21,22,23).

** Second, Appellant remarked (at Brief, page 5, lines 12-13) that

> *"However, Jost et al. do not teach etching **into**, but not through,* the substantially vertical component of the conductive layer as recited in claim 21... ". (underline added)

The above remark is confusing and is understood as Jost et al do not teach the step of " etching a contact hole in said overlayer and an overetch amount into but not through the substantially vertical component..." (as recited in claim 21).

** Appellant then mainly remarked (at Brief, page 5, third paragraph) that

> "...While Jost et al. teach an overetch into the conductive layer 40, it is noted that this overetch does not extend **into** the **vertical component** of their conductive layer, i.e., the substantially vertical component of layer 40 in the opening formed over the semiconductor layer. Rather, Jost et al. show that the etching of layer 44a extends only into the upper surface of conductive layer 40, not into the vertical component of the layer. See Fig. 11. As required by applicants' claims, the overetch amount is etched "*into* but not through the substantially **vertical component** of said layer of conductive material." See also applicants' Fig. 7 where it can be clearly seen that the overetch extends into the vertical component (localized thick region 34) of the conductive layer 26..."

** During patent examination, claims are given the broadest reasonable interpretation and limitations in the specification are not read into the claims (In re Yamamoto, 740 F.2d 1569, 222 USPQ 934 (Fed. Cir. 1984)). In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

At the beginning, it is noted that Appellant admitted "Jost et al. teach an *overetch* into the conductive layer 40". Appellant however alleged that "this overetch does not extend **into** the **vertical component** of their conductive layer, i.e., the substantially vertical component of layer 40 in the opening...".

In response, this is noted and found unconvincing. As clearly shown from Figure 10 to Figure 11 of Jost et al., an underlayer 40 having an opening is formed. A conductor layer 40 is formed over the underlayer 28 and in the opening, wherein the conductor layer 40 has a topography that includes substantially vertical component in the opening (the vertical component is formed in the opening, located along and adjacent to the sidewalls of the underlayer 28), which

conductor layer 40 also includes a horizontal component formed above the upper surface of the underlayer 28 (Figure 10). Etching a contact hole in the overlayer 44a and in an overetch amount into the substantially vertical component of the conductive layer 40 is further shown in Figure 11 of Jost et al.

As can be explicitly seen in from Figure 10 to Figure 11 of Jost et al, due to overetching into the substantial vertical component located adjacent to sidewalls of the underlayer 28, ***the vertical component of the conductive layer 40 is over-etched and in an overetch amount into the vertical component*** so that the remaining ***vertical component is recessed*** *down below the upper surface of the underlayer 28*, wherein the overetching is not extending entirely through the vertical component. Indeed, after overetching of the contact hole, a portion of the vertical component of the conductive layer 40 is still remained in the opening and below the underlayer 28 top surface.

Appellant alleged about applicant's Fig. 7 where it can be clearly seen that the overetch extends into the vertical component.

It is noted applicant's Fig. 7; however, attention is also directed to the subject matter of Appellant as also shown in **Figure 8 and Figure 9**. As can be seen, the conductive layer 40 (as shown in Figure 10) of Jost et al. is corresponding to the conductive layer 26 (as shown in Figure 8) of the Appellant's application. The vertical component 34 as shown in Figure 9 of Appellant's application is corresponding to the remaining vertical component of the conductive layer 40 of Jost et al after etching (Fig 11). Although a portion of the horizontal component of the conductive layer 40 (Figure 11 in Jost et al.) and a portion of the horizontal component of the conductive layer 26 (Figure 9 of Appellant) are being etched through, these vertical components as shown in Figure 11 of Jost et al. and as shown in Figure 9 of Appellant are not being etched through, since a portion of these vertical components are still remained in the opening of the underlayer, wherein these vertical components as localized thick regions are formed as the spacers (re further claims 22-23, noted Figs 8-9 and specification page 11, lines 5-29 disclosed that "*the localized thick region is formed as a spacer*" 34. Therefore, Jost clearly teach the claimed subject matter that requires *both* the etching extend **into** the vertical component *and* that it does not extend entirely **through** the vertical component", wherein Figure clearly shows 11, the vertical component of the conductive layer 40 is over-etched and in an overetch amount into

the vertical component so that the vertical component is **recessed** down below the upper surface of the underlayer 28, but not through the vertical component.

Re further claim 25, as already of record, Jost et al. explicitly disclosed (at col 4, line 58 through col 5) that "...cell polysilicon layer 40 and underlying cell dielectric layer 38 are patterned and etched to define the desired configuration of cell poly layer 40 for *capacitor* and interconnecting...".

Accordingly, it is believed that the rejection are outstanding and should be sustained.

(3) Rejection of claims 21-25 and 31-32 under 35 U.S.C. 102(e) by using Jun (5,459,094):

Appellant remarked (at Brief, page 7, third paragraph) that

> "...As interpreted by the Examiner, Jun teaches an "underlayer" 12 and an "overlayer" 17. However, applicants wish to point out that Jun teaches no layer of conductive material formed over the "underlayer" 12 as required in claim 21. Rather, conductive layer 16 is formed over insulating layer 14. Assuming that insulating layer 14 could be interpreted as an "underlayer," applicants wish to point out that insulating layer 14 is clearly greater in thickness than "overlayer" 17. See Fig. 4b..., the overlayer must have a thickness **greater** than the underlayer...".

In response, this is noted and found unconvincing. As clearly shown in Figures 4b-4c and 8a-8f, the conductive layer 16 is formed both *over* the underlayer 12 and *over* the insulating layer 14. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). The comprising-type claim does not preclude the claim from having other layers formed between the conductive layer 16 and the underlayer 12. In otherworld, the underlayer can be a composite stack or comprised a plurality of sub-underlayers.

Regarding a greater thickness, as already of record, Jun teaches forming the overlayer 17 having a thickness of about 1000 Angstroms (at col 5, lines 26-30; 17 in Fig 4b-4c; 25 in Figs 8b-8c). Jun also teaches forming the underlayer 12 (Fig 2, 8a-8c, 4a-4c) having a thickness of

about 100-200 Angstroms (column 4, lines 55-58). Accordingly, the overlayer of 1000 Angstroms (17, 25) has a thickness greater than the underlayer 12 of 100-200 Angstroms.

*** Applicant further remarked (at Appeal remark page 7, fourth paragraph) that "

> "Applicants further wish to point out that Jun does not teach etching a contact hole in the overlayer in an overetch amount into, but not through the substantially vertical component of the conductive layer as claimed. While Jun et al. teach etching into the surface of conductive layer 16, this etching does not extend into the substantially vertical component of the conductive layer. See Fig. 4c."

In response, attention is also directed to subject matter of Appellant's application as shown in **Figures 15-16**, since Figures 15-16 show "a structure having an opening *in* said at least one *semiconductor* layer" as recited in claim 31. As claimed in claim 31, as shown in Figures 11-16, and as described in the specification page 14, lines 19-35, and lines 9, line 29 through page 14, a substrate 52 having at least a semiconductor layer 58 (Figure 11) is provided. A structure having an opening 68 (Figs 12-13) is formed in the at least one semiconductor layer 58. A layer 80 of conductive material is formed over the at least one semiconductor layer 58 and filling the opening 68 with the conductive material to form a substantially vertical component 86 in the opening (Figs 14-15; specification page 13, lines 19-31). An overlayer 88 is formed (Fig. 15). A contact hole 92 is formed in the overlayer 88 and *extending into the vertical component 86 of the layer 80 of conductive material,* the contact hole disposed adjacent to and directly contacting the vertical component 86 in the opening (Figs 15,14). The contact hole is filled with a conducting material 95 (Fig 16).

Applicant's above remarks that "...Jun does not teach etching a contact hole in the overlayer in an overetch amount into, but not through the substantially vertical component of the conductive layer..." are noted and found unconvincing. Since, etching a contact hole in the overlayer 17 and an overetch amount into but not through the substantially vertical component of the layer 16 of conductive material in the opening is clearly shown Figures 4c, 8c-8f of Jun (col 5, lines 31+). Instead of ending on the conductive layer 16, the etching of the contact hole is continued to over-etch the conductive layer 16 and in an overetching amount into the vertical

component of the conductive layer 16, but not through the substantial vertical component (Figures 4c,8c-8f of Jun).

Especially, as similar to claim 21, claim 31 also recites "forming a contact hole in said overlayer and **extending into** said **vertical component** of said layer of conductive material...". As shown in **Figures 15,16** of Appellant's application, the surface of the conductive layer 80 (Fig 15) is etched, and this contact hole etching is defined by Appellant that it is extending into the substantially vertical component 86 of the conductive layer 80 in the opening 68 formed in the at least one semiconductor layer 58 (**also note specification page 14, lines 27-35**).

Accordingly, in the above rejection of claims 21 and 31, Jun anticipatively teaches (at Figures 4a-4f; 8a-8f) forming an underlayer 12 of a structure having an opening 15 in the at least one semiconductor layer 13 (Figs 4a,8a; col 5, lines 1-14); filling the opening 15 with the layer 16 of conductive material to form a substantially vertical component in the opening in the at least one semiconductive layer 13; forming an overlayer (17 in Fig 4b-4c; 25 in Figs 8b-8c) over the layer 16 of conductive material; and forming a contact hole in the overlayer and in an overetch amount extending into the vertical component of the layer 16 of conductive material in the opening, but not through, the contact hole disposed adjacent to and directly contacting the vertical component in the opening (Fig 4c;8c; col 5, lines 31-57; col 11, lines 44-55). Also, as already of record, Jun teaches the claimed limitations as recited in dependent claims 22-25,32.

Overetching an amount extending into the vertical component but not through the conductive layer as claimed and as also shown by Appellant's invention is the same as overetching an amount extending into the vertical component but not through the conductive layer as clearly disclosed by Jun. During patent examination, claims are given the broadest reasonable interpretation and limitations in the specification are not read into the claims (In re Yamamoto, 740 F.2d 1569, 222 USPQ 934 (Fed. Cir. 1984)). In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000).

Accordingly, it is believed that the rejection are outstanding and should be sustained.

(4) Rejection of claims 21-25 and 31-32 under 35 U.S.C. 103(a) over Bergemont (US 5,484,741) taken with Toshiyuki et al. (JP-05-109905) and Zamanian (US 5,793,111).):

This ground of rejection has been withdrawn by the examiner as cumulative.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Primary Examiner
Michael Trinh

Conferees:

SPE Zandra Smith

SPE Drew Dunn